

General Processor Information

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(DISCLAIMER: SPEC performance numbers are the highest rated for a given processor version. Actual performance depends on the computer configuration, and may be less, even significantly less than, the numbers given here. Also note that non-italicized numbers may be company estimates of performance when actual numbers are not available)

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
					int	fp			kB	Assoc				peak	typ		
Intel x86	8086	[vi]	78	v/16	5	-	-	1/1	1/1/na	-	-	5.0	3.0				0.029
					8	-	-										
					10	-	-										
	8088	[vi]	79	v/16	5	-	-	1/1	1/1/na	-	-	5.0	3.0				0.029
					8	-	-										
	80186	[vi]	82	v/16		-	-	1/1	1/1/na	-	-	5.0	1.5				
	80286	[vi]	82	v/16	6	-	-	1/1	1/1/na	-	-	5.0	1.5				0.134
					10	-	-										
					12	-	-										
	i386DX	[vi]	85	v/32	16			1/1		-	-	5.0	1.5				0.275
			87		20												
			88		25	6.5	1.9										
			89		33	8.4	3.0										
	i386SX	[vi,41]	88	v/32	16	2.4	0.9	1/1	4/na/na	-	-	5.0	1.5				0.275
		[vi]	89		20	3.5	1.3										
			89		25	4.6	1.9										
			92		33	6.2	3.3										
	i386SL	[vi]	90	v/32	20	3.5	1.3	1/1	4/na/na	-	-	5.0	1.0	2			0.855
91			25		4.6	1.9											

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)	
					int	fp			kB	Assoc				peak	typ			
Intel x86	i486DX	[vi]	89	v/32	25	14.2	6.7	2/1	5/na/5?	8 u.	4	5.0	1.0	2			1.2	
		[vi,45]	90		33	18.6	8.5											
		[vi]	91		50	33.4	14.5						0.8	3	5.0	3.9		81
	i486SX	[vi]	91	v/32	16	9.3	4.3	2/1	5/na/5?			5.0	1.0	2			1.185	
		[vi]			20	11.5	5.2											
		[vi]			25	14.2	6.7											
		[vi]	92	33	18.6	8.5	0.8	3				0.9						
	i486SL	[vi]	92	v/32	20	11.5	5.2	2/1	5/na/5?				0.8	3			1.4	
					25	14.2	6.7											
					33	18.6	8.5											
	i486DX2	[vi]	92	v/32	50	29.9	14.2	2/1	5/na/5?	8 u.	4	5.0	0.8	3			81	1.2
		[vi,20]			66	39.6	18.8								7.0	4.9		
	i486DX4	[vi]	94	v/32	75	41.3	20.1	2/1	5/na/5?	16 u.	4?	3.3	0.6	4			345	1.6
		[vi,42]			100	55	27									4		
	P5	[vi]	93	v/32	60	70.4	55.1	3/2	5/na/8	8/8	2/2	5.0	0.8	3			296	3.1
[2,10]		93	66		78	63.6	16.0											

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{eh} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)			
					int	fp	int	fp			kB	Assoc				peak	typ					
Intel x86	P54VRT (Mobile)	[vi,sp]	94	v/32	75	89.1	68.5	2.4	2.1	3/2	5/na/8	8/8	2/2	2.9	0.6	4	5.2	2.4	3.1			
		[vi,sp]	94		90	110	84.4	2.9	2.5								6.5	3.0				
		[vi]	96		120	157	108	3.8	3.0													
		[mr,vi]	96		133	174	121	4.2	3.3									3.3				
		[vi]	96		150			4.6	3.3									3.8				
	P54C	[2,11,vi]	94	v/32	100	122	93.2	3.3	2.8	3/2	5/na/8	8/8	2/2	3.3	0.6	4	5.0		148	3.1		
	P54CQS	[47,vi]	95	v/32	120	157	108	3.8	3.0	3/2	5/na/8	8/8	2/2	3.3	0.35	4	10.0		90	3.1		
	P54CS	[53,vi]	95	v/32	133	174	121	4.2	3.3	3/2	5/na/8	8/8	2/2	3.3	0.35	4			90	3.1		
		[31,vi]	96		150	181	125	4.3	3.3													
		[vi]			166	198	138	4.8	3.7													
		[vi]			200			5.5	4.2									3.45				
	P55C (MMX)	[vi]	97	v/32	166			5.6	4.3	5/2	6/na/8	16/16	4/4	2.8	0.35	4			141	4.5		
		[vi]			200			6.4	4.7									15.7				
		[vi]			233			7.1	5.2									17				
		[vi]			266																	
	P55VRT (Mobile MMX)	[vi]	97	v/32	166			5.6	4.3	5/2	6/na/8	16/16	4/4	2.45	0.35	4	7.8		141	4.5		
		[vi]	97		166																2.9	
		[vi]			200			6.4	4.7								1.8	0.25			?	3.4
		[vi]			233			7.1	5.2								2.0					3.9
		[vi]			98	266																
P6 (Pentium Pro)	[vi]	95	v/32	150	245	220	6.1	5.4	7/?	14/14/16 ^(D)	8/8 ^(L)	4/2	3.1	0.6	4	29.2	23.2	306 ^(L)	5.5			
				180			7.3	6.1					3.3	0.35	4			195 ^(L)				
				200	320	283	8.2	6.8					3.3	0.35	4	35	28.1					
	[vi]	96		166	293	261	7.3	6.2	7/?	14/14/16 ^(D)	8/8 ^(M)	4/2	3.3	0.35	4	29.4	23.4	195 ^(M)				
				200			8.7	6.7					3.3	0.35	4							
				200			8.7	6.8					3.3	0.35	4			195 ^(N)				

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)				
					int	fp			kB	Assoc				peak	typ						
Intel x86	Pentium II (Klamath)	[vi]	97	v/32	233	9.5	6.4	7/?	16/16	4/4	2.8	0.35	4			203	7.5				
		[vi]			266	10.8	6.9														
		[vi,is97,sp]			300	11.9	8.6														
	Pentium II (Deschutes)	[vi]	98		333	13.0	9.6							2.2	0.25						131
		[vi,by]			350	13.9	11.2														
		[vi]			400	15.8	12.4														
		[vi,is98]			450	17.2	12.9														
	Mobile Pentium II (Deschutes)	[vi]	98		233	9.5	6.4								0.25						131
		[vi]			266	10.8	6.9														
		[th]			300	11.9	8.6														
	Celeron (Deschutes)	[vi]	98		266	10.8	6.9								0.25				15.6		131
		[vi]			300	11.9	8.6														
	Pent II Xeon (Deschutes)	[vi]	98		400	16.5	13.7							2.0	0.25				23.3		131
		[vi]			450	18.9	14.7														
	Pent III (Katmai)	[vi]	99		v/32	450	18.7				13.7				2.0	0.25					
500				20.6		14.7															
550				22.2		15.0															
600				24.0		15.9															
Pent III Xeon (Katmai)	[vi]	99	v/32	500	20.6	14.7				2.0	0.25										
				550	22.2	15.0															

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
						int	fp			kB	Assoc				peak	typ		
Intel x86	Celeron (Mendocino)	[vi]	98	v/32	300	12.0	9.7			16/16 128	?? ?	2.0	0.25			17.5		19.0
					333	13.1	10.4									19.4		
			366		14.1	11.2	21.4											
			400		15.1	11.8	23.4											
			433		16.1	12.1												
			466		17.0	12.7												
			500		17.9	12.9												
			533															
	Mobile Celeron (Mendocino)	[vi]	99	v/32	266					16/16 128	?? ?	1.6	0.25				7.0	18.9
					300	12.0	9.7									7.7		
					333	13.1	10.2									8.6		
					400											9.2		
	Mobile Pentium II (Dixon)	[vi]	99	v/32	266					16/16 256	?? ?	1.6	0.25				7.0	27.4
					300											7.7		
					333											8.6		
					366											9.5		
					400											8.7		
		[vi]	99		400						1.55			7.5				

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	Tech (um)	Met	Power (W)		Size (mm ²)	Xsistor (10 ⁶)	
						int	fp			kB	Assoc				peak	typ			
Intel x86	Pentium III (Coppermine)	[vi]	99	v/32	500					16/16 256	?? 8	1.6	0.18	6			106	28	
					533														
					550														
					600														
					650														
					667														
					700	33.0	29.0												
					733	35.6	30.4												
					800														
			1000																
			00																
		PentIII Xeon (Coppermine?)	[vi]	99	v/32	600				16/16 256	?? 8	1.6	0.18	6			106	28	
	667					33.0	29.0												
	733					35.6	30.4												
		Mobile Pentium III (Coppermine)	[vi]	99	v/32	400				16/16 256	?? 8		0.18	6			106	28	
	450																		
	500																		
	600/500																		
	650/500																		
	700/550																		
		Celeron (Coppermine)	[vi]	00	v/32	533				16/16 128	?? 4	1.5	0.18	6					
566																			
600																			

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	PR Rating	SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	Tech (um)	M _e t	Power (W)		Size (mm ²)	Xsistor (10 ⁶)			
							int	fp			kB	Assoc				peak	typ					
Cyrilx/ IBM x86	486SLC	[vi,cm]	92?	v/32	20				1/1									72	0.6			
		[vi]			33																	
	486DX4	[vi,cm]	93?	v/32	100				2/1		8 u.	4	3.0					196	1.1			
	5x86 (M1sc)	[vi]	95	v/32	100				2/1	6/6/?	16 u.	4	3.45	0.65	3	3.5	3	144	2.0			
		[vi]	95	v/32	120				2/1	6/6/?	16 u.	4	3.3	0.65	3			144	2.0			
	5gx86 (MediaGX)	[is96]	96	v/32	120				2/1	6/6/? ^(O)	16 u.	4	3.3	0.6	3			160	2.4			
		[vi]	97		133																	
		[vi]	97		150	PR150											0.5			3		
		[vi]	98		233																	
	6x86 (M1)	[46]	95	v/32	100				3/2	7/7/?	16 u.	4	3.3	0.65	3	10		394	3.0			
		[pn,vi]			120										5		210					
	6x86 (M1R)	[vi]	96	v/32	100	PR120			3/2	7/7/?	16 u.	4	3.3/ 2.8	0.5	5			169	3.0			
		[vi]			110	PR133																
		[vi]			120	PR150																
		[pn,vi]			133	PR166																
		[vi]			150	PR200															0.44	
	6x86MX (MII)	[vi]	97	v/32	150	PR166			3/2	7/7/?	64 u.	4	2.9	0.35	5			197	6.0			
		[vi,55]			166	PR200	~5.1	~2.2														
		[vi,55]			188	PR233		~2.7														
		[vi]	97		208	PR266																
[vi]		98	233		PR300												0.3			5		
[vi]		98	250		PR333																	
MXi (Cayenne)	[vi]	99?	v/32		PR300					64 u.			0.25	5			~90					
					PR400																	

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	T _{eh} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)	
						int	fp	int	fp			kB	Assoc				peak	typ			
Nexgen (AMD)	Nx586	[42,43]	95	v/32	93					5/1 ^(D)	7/9/na ^(D)	16/16		4.0	0.5	5	16	9	199	3.5	
		[vi]	95	v/32	133					5/1 ^(D)	7/9/? ^(D)	16/16		3.6	0.44	5			118		
AMD	386	[cm]	90																		
	Am486	[pn]	95	v/32	120					2/1					0.5	3		~3			
	Am5x86	[vi]	95	v/32	133					2/1		16 u.			0.35	3			43		
	Am5k86	[39,vi]	95	v/32	75	(PR75)				6/?	5/5/5?	16/8	4/4	3.5	0.35	3			161	4.3	
					90	(PR90)															
					100	(PR100)															
	K5	[39,vi]	96	v/32	90	(PR120)				6/?	5/5/5?	16/8	4/4	3.5	0.35	3		14	161	4.3	
					105	(PR133)															
					120	(PR166)															
	K6	[vi, is97, 55]	97	v/32	166					7/?	6/7/7 ^(D)	32/32	2/2	2.9	0.35	5		17.2	10.3	162	8.8
					200			~6.2	~3.5								20	12			
					233			~6.8	~3.8								28.3	17			
					266																
					266																
					300																
		[by]																			
	[vi]												0.25	5				68	8.8		
	[vi]	98																			
K6-2 (K6-3D)	[vi]	98	v/32	266					7/?	6/7/7 ^(D)	32/32	2/2		0.25	5				81	9.3	
				300																	
				333																	
				350																	
				400																	
				450																	
				475																	
				500																	
				533																	
				550																	

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	Tech (um)	Met	Power (W)		Size (mm ²)	Xsistor (10 ⁶)		
						int	fp	int	fp			kB	Assoc				peak	typ				
IDT	WinChip (C6)	[vi,55]	97	v/32	200			~4.1	~2	3/1 ^(D)	5/5/?	32/32	2/2	3.3	0.35	4			88	5.4		
		[vi]			225													3.5				
		[vi]			240																	
	WinChip2 (C6+)	[vi]	98	v/32	200					6/2-	6/6/?	32/32	2/4	3.3	0.25	5			58	5.8		
		[vi]			225																	
		[vi]			233																	
		[vi]			240													3.5				
		[vi]			266																	
		[vi]			300																	
	<i>IDT's Centaur division was acquired by VIA, eliminating plans for WinChip3 and WinChip4</i>																					

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	Tech (um)	Met	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
						int	fp	int	fp			kB	Assoc				peak	typ		
Mot 68k	68020	[45]	85	v/32	25	NA	NA			1/1	?/na/na	NA/.25	NA/1	5.0	1.5	2				
	68030	[41,45]		v/32	50		NA			1/1	3/na/na	.25/.25	1/1	5.0	1.2	2			55	0.27
	68040	[10,45]	89	v/32	25	21	15			2/1	6/na/6	4/4	4/4	5.0	0.8	3	6.0		164	1.2
		[vi]	94?	v/32	66															
68060	[15,21]	93	v/32	50	~60 ^(B)	~45 ^(B)			3/2	8/na/8	8/8	4/4	3.3	0.5	3	3.9		198	2.4	

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ec} h (um)	M _e t	Power (W)		Size (mm ²)	Xsistor (10 ⁶)					
					int	fp	int	fp			kB	Assoc				peak	typ							
Power PC	601	[15,25]	93	32	50	40	60			4/3	4/5/6	32 u.	8	3.6	0.6	4	9.1	6.5	121	2.8				
	601v	[9,vi]	94	32	100	105	125			4/3	4/5/6	32 u.	8	3.3	0.5	5	5.6	4.0	74	2.8				
		[vi]	95		120																			
	602	[43]	95	32	66	40				4/2	4/5/6?	4/4	2/2	3.3	0.5	4		1.2	50	1.0				
	603	[2,6,25]	94	32	80	75	85			4/2	4/5/6	8/8	2/2	3.3	0.5	4	3.0	2.2	85	1.6				
	603e	[44, vi]	95	32	100	120	105			4/2	4/5/6	16/16	4/4	3.3	0.5	4	3.5		98	2.6				
			96		200			5.3	4.0										80					
		[vi]	97		240			6.3	4.6					2.5	0.35	5	5.5		42					
					250																			
					275																			
					300			7.4	6.1													~3.5		
	603q	[vi]	96	32	160	120	84			2/1	5/5/5?	16/8	4/2	3.3	0.5	3		1.2	69					
	604	[7,8,vi]	94	32	100	128 ^(H)	120 ^(H)	3.6	3.2	6/4-	4/5/6	16/16	4/4	3.3	0.5	4		14	197	3.6				
		[53,vi,sp]	95		133	176 ^(H)	157 ^(H)	4.7	3.8									17.5						
		[vi]	96		180			6.2	5.3															
	604e	[mw,vi]	96	32	166			6.7	6.3	6/4-	4/5/6	32/32	4/4	2.5	0.5	5	15	10	148	5.1				
		[sp]			200			9.3	8.9												19.5	12		
		[vi]			225			10.2	7.6															
		[vi]	97		200			9.3	8.9								1.9	0.35			5	16	14.5	96
		[vi]			233			10.3	7.3															~15
[vi]		250					11.1	7.8																6
[vi]		300					12.9	8.5								12			6.8			47		
[vi]		333				13.9	8.6									7.5								
[vi]		350				14.6	9.0									8								
[vi]		375				15.9	10.1																	

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	Tech (um)	Met	Power (W)		Size (mm ²)	Xsistor (10 ⁶)	
					int	fp	int	fp			kB	Assoc				peak	typ			
Power PC	RS64	[vi-ibm]	98	64	125						64/64									
	RS64-II	[vi-ibm]	98	64	262				5/4		64/64									
	630 (Power3)	[vi]	98	64	200			13.2	30.1	8/5	5?/5?/?	32/64	128/128	0.25	5			270		
		[vi]	99		222															
		[vi]	00		440													160		
	7400 (G4)	[vi-mot]	99	64	350					7/3-		32/32		1.8	0.15	6			83	6.5
					400												8.0	5.0		
450							21.4	20.4												
500																				
Power	P2SC	[vi]	97	32	120			5.6	16.6	10/6-		32/128		2.5	0.29	5			335	15
		[vi]	97		135			6.2	17.6								30			
		[vi]	98		160			8.6	26.6											

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)	
					int	fp	int	fp			kB	Assoc				peak	typ			
Sparc	CY7C601	[19,20]	90?	32	40	21.8	22.8			1/1	5/na/na	na/na	na/na	5	0.8	2	3			
	Weitek 2x	[20]	92?	32	80	32.2	31.1			1/1		16/8			0.8				1.8	
	Micro	[20,41]	91?	32	50	26.4	21.0			1/1		4/2		5	0.8	2	4		225	
	Micro 2	[20,37]	94	32	85	65.3	54.6			1/1	5/na/5?	16/8			0.5	3		233	2.3	
		[vi]	95	32	110	79	65	1.6	2.0						0.4	3	9			
	Micro 3		97	64																
	Hyper (Ross)	[20]	93?	32	72	80	105			4/2-	6/6/6	8/na	?/na		0.8					
		[37]	94	32	100	112	127			4/2-	6/6/6	8/na	?/na		0.5	3			327 ^(C)	1.7 ^(C)
		[49]	95	32	125	159	183			4/2-	6/6/6	8/na	?/na		0.4					
		[pn,vi]	95	32	150	180	245	4.1	4.9	4/2-	6/6/6	8/na	?/na		0.4					
		[pn,vi]	96	32	200	235		5.3	5.1	4/2-	6/6/6	16/16			0.35					
	Super	[10,20,vi]	92	32	60	89	103	~1.5	~1.7	5/3	4/4/5	20/16	5/4	5.3	0.6	3	14.2		256	3.1
	Super 2	[29,37,vi]	95	32	75			3.1	3.1	5/3	4/4/5	20/16	5/4	5?	0.6	3			299	3.1
90					135	147	~3.5	~3.5									16			
Thunder 1	[21]	93	32	50	120	240			8/4				5	0.6					~6	

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
						int	fp	int	fp			kB	Assoc				peak	typ		
Alpha	21064	[vi]	92	64	100	75	95	1.9	2.8	4/2-	7/7/10	8/8	1/1	3.3	0.75			234	1.68	
		[vi]			133	75	112													
		[vi]			150	84	128	2.2	3.7											
		[vi]			166	116	135	3.0	3.6											
		[vi]			175	114	162													
		[1,4,23]			200	138	200													
	21064a	[vi]	94	64	225	163	231	3.7	5.7	4/2-	7/7/10	16/16	1/1	3.3	0.5	4			164	2.8
		[vi]			233	165	223	4.3												
		[vi]			266	199	263	5.2	6.3											
		[18,23]			275	203	293	5.2	6.3											
		[vi]	95	300	220	300	5.2	6.5												
	21066a	[vi]	93	64	166	77	110			4?/2-	7/7/10	8/8	1/1	3.3	0.5	4			161	1.75
		[vi]	94		225	135	205													
		[34,37]			233															
		[vi]			275	170	240													
	21164	[vi]	94	64	266	329	429	7.9	11.8	4/4-	7/7/9	8/8 96	1/1 ?	3.3	0.5	4			299	9.3
		[22,21]			300	341	513	8.5	12.7											
		[vi]	95		333	412	542	9.8	13.4											
	21164PC	[vi,is97]	97	64	400					4/4-	7/7/9	16/8	1/1	2.5	0.35	4			138	3.5
		[vi]	97		466			14.6	17.4											
		[vi]	97		533			16.1	18.8											
[vi]		97	600				17.9	19.9												
21164a	[vi]	96	64	400	~500	~750	12.3	17.2	4/4-	7/7/9	8/8 96	1/1 ?	2.0	0.35	4			209	9.3	
	[vi]	96		433			13.9	18.1												

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d/L2)		V _{dd} (V)	Tech (um)	Met	Power (W)		Size (mm ²)	Xsistor (10 ⁶)					
						int	fp	int	fp			kB	Assoc				peak	typ							
Alpha	21264	[vi]	98	64	575			30.3	47.7	6/4	7/7/10	64/64	2/2	2	0.35	6	~60		302	15.2					
		[vi,is97]	98		667			44	66								72								
		[vi]	98		700																				
	21264PC	[by]	98	64						6/4	7/7/10				0.25										
	21264a	[cg,by]	98	64	800					6/4	7/7/10				0.35										
		[vi]	99																			0.25			
		[vi]	00																			0.18			
	21364	[cg,by]	00		1000			~70	~120	6?/4	6/6/?	64/64 1500	2/2 6	1.5	0.18	6	100		350	100					
21464	[cg]	03												0.18						~250					

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)	
					int	fp	int	fp			kB	Assoc				peak	typ			
MIPS	R2000	[mc]	86	32															0.11	
	R3000	[12,20]	88	32	40	27.9	35.8			1/1	5/na/na	na/na	na/na	5.0	1.2		4.0			
	R6000 ^(E)	[20,32]	91	32	66.7	40.6	45.1			1/1	5?/na/na	na/na	na/na						(E)	
	R4000	[20,32]	92	64	100	59	61			2/1	8/na/10	8/8	1/1		1.0				213	1.1
	R4200	[2,5]	93?	64	80	55	30			1/1	5/na/5	16/8	1/1	3.3	0.64	3	1.8	1.5	78	1.4
	R4300i	[52]	95	64	100	60	45			1/1	5/na/5	16/8	1?/1?	3.3	0.35	3		1.8	45	1.7
		[vi]	96	64	133												2.2			
	R4400	[10,17,sp]	92	64	150	109	97			2/1?	8/na/10	16/16	1/1	3.3	0.6	3	15		186	2.3
		[37,38]	94	64	200	146	143	4.3	?						0.5	2			148	2.2
		[53,sp]	95	64	250	180	178	5.1							0.35				108	~2.2
	R4600	[13,37]	94	64	150	114	83			2/1	5/na/5	16/16	2/2	3.3	0.64	3	4.6	3.0	77	1.85
	R4700	[37,vi]	95	64	175	132	105			2/1	5/na/5	16/16		3.3	0.6	3	3.5		73	1.85
	R5000	[sp]	96	64	180			4.8	5.4	3/2-	5/na/8	32/32	2/2	3.3	0.35	3			84	3.6
		[vi]	96		200			5.5	5.5								10			
		[vi]	96		250															
	R5000A	[vi]	97	64																
	RM5271	[vi]	99	64	300									0.25						
RM7000	[vi]	97	64	300			~13	~15	?/2		16/16	4/4		0.25	4	13		80		
R8000	[20,37]	94	64	75	112	311			6/4-	5/5/?	16/16	1/1	3.3	0.7	3			596 ^(C)	3.43 ^(C)	
	[vi]	95	64	90	132	396								0.5		~30				

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
						int	fp	int	fp			kB	Assoc				peak	typ		
MIPS	R10000	[vi]	96	64	180			10.3	15.6	5/4	5/6/7	32/32	2/2	3.3	0.35	4	~30	298	6.8	
		[vi]	96		195	300	600	11.4	19.1											
		[vi]	98		250			14.7	24.5											
		[vi]	98?		275			>12	>24											
	R12000	[vi]	98	64	270			15.8	25.2											
					300			18.4	34.4											
	H1	[vi]	00																	
H2	[vi]	01																		

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
						int	fp	int	fp			kB	Assoc				peak	typ		
ARM	610	[3,15,27]	93	32	25	16	NA			1/1	3/na/na	4 u.	64	5.0	1.0	2	0.5		71	0.36
	710	[27]	94	32	33		NA			1/1	3/na/na	8 u.	4	5.0	0.8	2	0.5		46	0.54
	810	[vi]	96	32	75		NA			1/1	5/na/na	8 u.	4?	3.3	0.5	3	0.5?			
	SA-110	[vi,is96]	96	32	160		NA			1/1	5/na/na	16/16	32/32	1.65	0.35	3		0.5	50	2.1
					200		NA							2.0				0.9		
					96	32	233		NA											
	SA-1100	[vi]	97	32	133		NA			1/1	5/na/na	16/8	32/32	1.5	0.35	3	0.3	0.2		2.5
					200		NA										0.45	0.25		
940T	[vi]	98	32	150		NA			1/1	5/na/na	4/4	64/64	3	0.35		0.68		15		
1020T	[vi]	00	32	300								32/32		0.25						

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	T _{ch} (um)	M _{et}	Power (W)		Size (mm ²)	Xsistor (10 ⁶)		
					int	fp	int	fp			kB	Assoc				peak	typ				
Hobbit	92010	[3,15]	92	32	20	8	NA			1/1	3/na/na			3.3	0.9		0.25				
	92020S	[40]	94	32			NA														
PA-RISC	7000	[32,54]	89	32	50			1.6	2.0	1/1	5/na/na	na/na	na/na								
			91		66	51	82								1.0			196	0.58		
	HARP-1	[41]		32	120	70	120														
	7100	[3,10,sp]	92	32	100	124	159	3.2	4.0	2/2-	5/na/6	na/na	na/na	5.0	0.8	3	23.0		202	0.85	
	7150	[24,sp]	94?	32	125	149	201	5.2	4.6	2/2-	5/na/6?	na/na	na/na	5.0	0.8	3	30		196	0.85	
	7100LC	[24]	94	32	100	119	137	4.6	4.7	3/2	5/na/6?	1/na	?/na	5.0	0.8	3	~10		196	0.8	
	7200	[24]	94	32	120	~150	~250	6.4	9.1	3/2	5/na/6?	na/2	na/64	4.4	0.55	3	30		210	1.26	
	7300LC	[vi]	96	32	160	~200	~275	7.8	7.6	3/2	5/na/6?	64/64	2/2		0.5	3	15		259	9	
	8000	[33,48]	96	64	180	>400	>600	11.8	20.2	10/4-	7/9/9	na/na	na/na		0.5	4	>40		345	3.9	
	8200	[vi]	97	64	220			15.5	25					3.3	0.5	5				3.8	
	8500	[vi]	98	64	360					?/4		1M / 0.5M	4/4		0.25					140	
					440			34	~52												
	8600	[vi]	00	64	550																
	8700	[vi]	01	64	800										0.18						
	8800	[vi]	02?	64																	
8900	[vi]	03?	64																		
SH Hitachi	II	[21]	93	16/32	28.7	~8	NA			1/1	5/5/na	4 u.	4	5	0.8	3	0.4		~200		
	7708 (III)	[21]	94	16/32	60	~35	NA			1/1	5/5/na	8 u.	4	3.3	0.5	3	0.6		44	0.8	
	7709 (III)	[vi]	97	16/32	80					1/1	5/5/na	8 u.	4	3.3	0.35			0.26			
	7750 (IV)	[vi]	97	16/32	200					2?/2		8/16		1.8	0.25			1.5			

Processor	Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V _{dd} (V)	Tech (um)	Met	Power (W)		Size (mm ²)	Xsistor (10 ⁶)
					int	fp	int	fp			kB	Assoc				peak	typ		
not available yet.																			

Power: peak power numbers used when available, else estimated from average power. Easier to find peak, rather than average.
Units: Functional units NOT including “system” unit; **Issue:** Peak instructions issued per cycle; “-”: Indicates limitations on peak issue rate. **Cache:** On-chip cache (except where footnoted).

SPEC: Numbers that are in *Italics* indicate official CINT95 and CFP95 numbers registered with SPEC (these are peak, not base).

B: Estimated that x60 is 3 times the performance of the x40.

C: Combined total for 2 chips.

D: Data for the RISC-like core. (AMD: rops; NextGen: RISC86 instructions; Intel: uops; IDT: micro-instructions)

E: This was an ECL implementation of the MIPS II ISA..

F: External (in an MCM package)

G: Single-chip CPU / Combined MCM package.

H: These are the highest SPEC numbers reported so far for the 604, which fall below the original estimates (100MHz - 160/165; 133MHz - 200/200)

J: This chip reportedly combines a Pentium and PPC604 on one chip (multiple die?).

L: This P6 has a 256kB L2 (15.5 million xsistors) in the same MCM package (but xsistors not counted in total).

M: This P6 has a 512kB L2 (31 million xsistors) in the same MCM package (but xsistors not counted in total).

N: This P6 has a 1MB L2 (62 million xsistors) in the same MCM package (but xsistors not counted in total).

O: Includes an integrated on-chip graphics co-processor, but is not included in the unit/issue count.

SOURCES (* = Can be found on the CPU Info Center)

- [1] = ISSCC92
- [2] = ISSCC94
- [3] = Hot Chips IV
- [4]* = <http://netlib2.cs.utk.edu/performance/html/PDStop.html>
- [5]* = Preliminary Product Sheet for R4200
- [6] = to be published.
- [7]* = Press Release 4/19/94: 100MHz PPC604
- [8] = uP 4/94 (as reported by M. Horowitz)
- [9]* = Press Release 3/30/94: 100MHz PPC601
- [10] = Spectrum 12/93
- [11] = to be published.
- [12] = Courtesy M. Horowitz, SPEC Table
- [13]* = Product Sheet for R4600
- [15] = CompCon 93
- [16] = CompCon 94
- [17]* = Product sheet for R4400
- [18]* = DEC Press Release.
- [19] = CY7C601 Data Book
- [20] = SPECtable from John Dimarco.
- [21] = Hot Chips 94.
- [22]* = DEC Press Release 9/7/94
- [23]* = John DiMarco's SPEC Table.
- [24]* = HP's Online server (<http://www.wsg.hp.com/wsg/Strategy/strategy.html>)
- [25]* = PowerPC WhitePapers (http://www.austin.ibm.com/tech/p2ppc_tech.html)
- [27] = from Dave Jaggard, chief architect of the ARM.
- [30] = 10/10/94 EE Times
- [31]* = Computergram News
- [32] = A Guide to RISC Microprocessors. Michael Slater, 1992.
- [33]* = from comp.arch (http://infopad/~burd/gpp/announce/pa8000_overview)
- [34] = 11/21/94 EE Times
- [35] = Leslis Kohn, "Ultrasparc", Invited Speaker, Micro 27 Conf.
- [36] = from comp.arch -- Alain Lachapelle (alainl@cam.org)
- [37] = uP 12/26/94
- [38]* = MIPS Home Page (<http://www.mips.com>)
- [39] = uP 10/24/94
- [40] = uP 1/24/94
- [41]* = CHIPS and SYSTEMS SPEC Chart, by Gary Snow.
(http://infopad.eecs.berkeley.edu/~burd/gpp/summary/snow_survey)
- [42]* = CHIPLIST 7.2 by Aad Offerman
(<http://einstein.et.tudelft.nl/~offermand/chiplist.html>)
- [43] = ISSCC95
- [44] = Motorola PPC Home Page:
(<http://www.mot.com/PowerPC/prodinfo.html>)
- [45] = Advanced Microprocessors, Daniel Tabak, 1991
- [46] = uP 2/16/94
- [47]* = Intel Press Release
- [48] = Compcon 95.
- [49] = Electronic News 3/20/95
- [52]* = Press Release 4/17/95
- [53] = uP 6/19/95
- [54] = A Practitioner's Guide to RISC Microprocessor Architecture, Patrick Stakem, 1996
- [55] = http://www.heise.de/ct/art_ab97/9715spec
- [vi] = Vendor Info
- [vp]* = Vendor Press Release
- [pn]* = PowerPC News
- [mw] = MacWeek (online)
- [by] = Byte
- [bw] = Business Wire
- [mr] = Microprocessor Report
- [sp] = SPEC
- [is##] = ISSCC, where the ## indicates the year.
- [cg] = Computergram International
- [th]* = Tom's Hardware Guide
<http://www2.tomshardware.com/irm298.html>
- [re] = The Register <http://www.theregister.co.uk>

NOTE: Hobbit & ARM SPEC calculated from 28k Drystones ~ = 8 SPECint92

Hobbit = 27k Dry @ 20 MHz

ARM6 = 28k Dry @ 20 MHz